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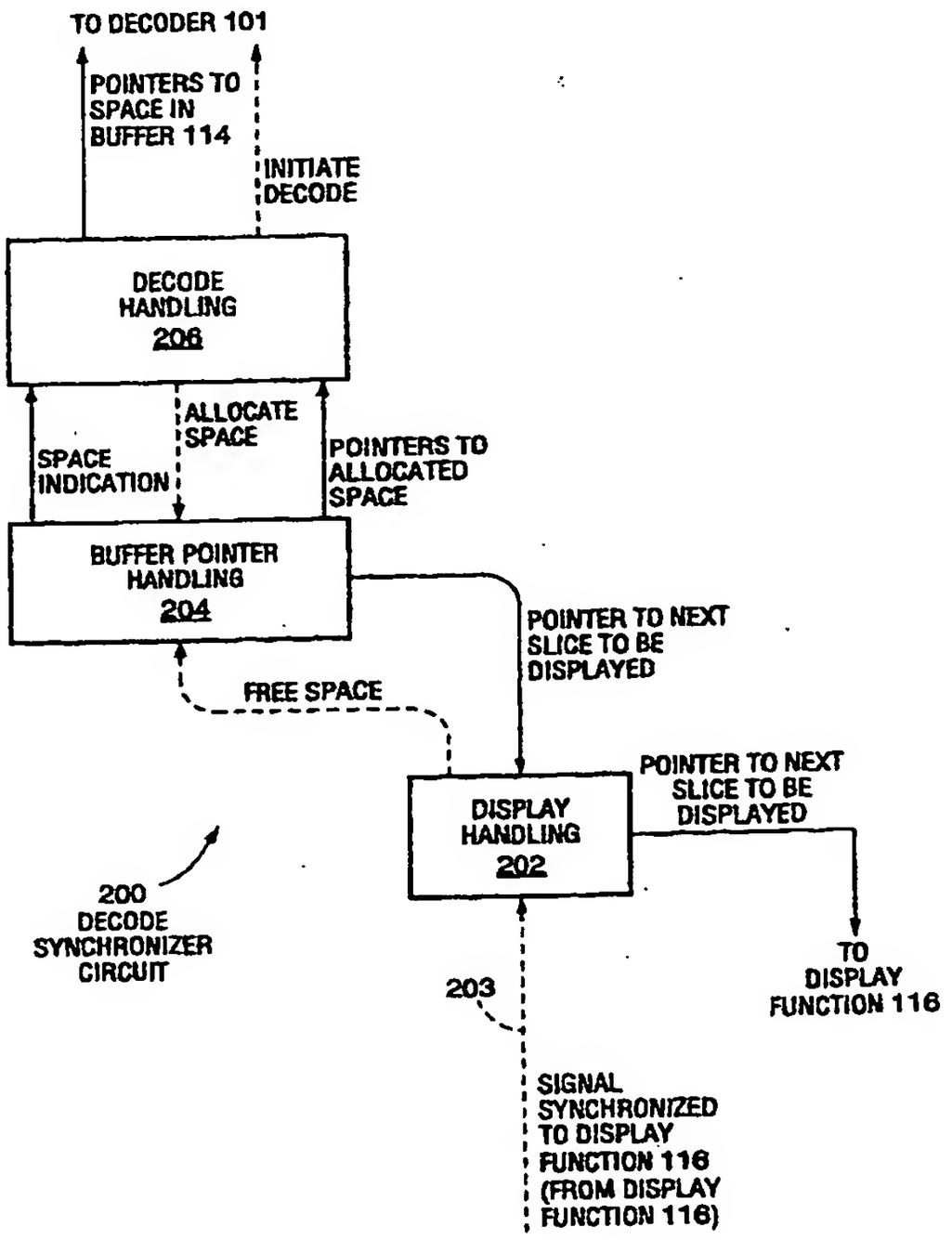
(54) Title: VIDEO DECODER WITH REDUCED SIZE DISPLAY BUFFER

(57) Abstract

A decoder system is provided for decoding an input video signal. A buffer memory holds slices of reconstructed B–pictures for display. The decoder is controlled in accordance with an amount of available memory in the buffer (the amount of available memory in the buffer depends both on how much data has been decoded and also upon how much data has been displayed). In addition, a buffer memory input controller controls into which locations of the buffer memory the slices of the reconstructed B–pictures are stored. As a result, only 2.53 frames of buffer memory are required.



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VIDEO DECODER WITH REDUCED SIZE DISPLAY BUFFER

Technical Field

The present invention relates to decoder systems for decoding MPEG-encoded video data for display and, in particular, to a decoder system that can decode MPEG-encoded video data for display employing only 2.53 frames of display buffer.

Background

Advances in audio and video compression and decompression techniques, together with very large scale integration technology, have enabled the creation of new capabilities and markets. These include the storage of digital audio and video in computers and on small optical discs, as well as the transmission of digital audio and video signals from direct broadcast satellites.

Such advances were made possible, in part, by international standards which provide compatibility between different approaches to compression and decompression. One such standard is known as "JPEG," for Joint Photographic Expert Group. A later developed standard is known as "MPEG 1." This was the first set of standards agreed to by the Moving Pictures Expert Group. Yet another standard is known as "ITU-T H.261", which is a video compression standard particularly useful for video teleconferencing. Although each standard is designed for a specific application, all of the standards have much in common.

MPEG 1 was designed for storing and distributing audio and motion video, with emphasis on video quality. Its features include random access, fast forward and reverse playback. MPEG 1 serves as the basis for video

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CD's and for many video games. The original channel bandwidth and image resolution for MPEG 1 were established based upon the then available recording media available. The goal of MPEG 1 was the reproduction of recorded digital audio and video using a 12 centimeter diameter optical disc with a bit rate of 1.416 Mbps, 1.15 Mbps of which is allocated to video.

The compressed bit streams generated under the MPEG 1 standard implicitly define the decompression algorithms to be used for such bit streams. The compression algorithms, however, can vary within the specifications of the MPEG 1 standard, thereby allowing the possibility of a proprietary advantage in regard to the generation of compressed bit streams.

A later developed standard known as "MPEG 2" extends the basic concepts of MPEG 1 to cover a wider range of applications. Although the primary application of the MPEG 2 standards is the all digital transmission of broadcast-quality video at bit rates of 4 Mbps to 9 Mbps, it appears that the MPEG 2 standard may also be useful for other applications, such as the storage of full length motion pictures on 12 centimeter diameter optical discs, with resolution at least as good as that presently provided by 12 inch diameter optical discs.

The MPEG 2 standard relies upon three types of coded pictures. I ("intra") pictures are fields or frames coded as a stand-alone still image. Such I pictures allow random access points within a video stream. As such, I pictures should occur about two times per second. I pictures should also be used where scene cuts (such as in a motion picture) occur.

P ("predicted") pictures are fields or frames coded relative to the nearest previous I or P picture, resulting in forward prediction processing. P pictures allow more compression than I pictures, through the use of motion compensation, and also serve as a reference for B pictures and future P pictures.

B ("bidirectional") pictures are fields or frames that use the closest past and future I or P picture as a reference, resulting in bidirectional prediction. B pictures provide the most compression and increased signal to

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noise ratio by averaging two pictures. The theory behind I, P and B pictures are more thoroughly described in U.S. Patent Nos. 5,386,234 and 5,481,553 assigned to Sony Corporation, which are incorporated herein by reference in their entirety.

A group of pictures ("GOP") is a series of one or more coded pictures which assist in random accessing and editing. A GOP value is configurable during the encoding process. Since the I pictures are closer together, the smaller the GOP value, the better the response to movement. The level of compression is, however, lower.

In a coded bitstream, a GOP must start with an I picture and may be followed by any number of I, P or B pictures in any order. In display order, a GOP must start with an I or B picture and end with an I or P picture. Thus, the smallest GOP size is a single I picture, with the largest size unlimited.

Fig. 1 is a block diagram illustrating a video decoder system 100, including a decoder 101. A coded bitstream 102 is input to a variable-length decoder (VLD) 104 of the decoder. The VLD 104 expands run/amplitude pairs of quantized frequency coefficients that are encoded into the bitstream 102. The frequency coefficients are then converted into the spatial domain using an inverse discrete cosine transform circuit 110. The resulting "error terms" indicate a content difference from a reference macroblock to another macroblock to be decoded (referred to herein as a "current macroblock").

Spatial differences from reference macroblocks to current macroblocks are encoded as two-dimensional motion vectors in the coded bitstream 102. Specifically, the two-dimensional motion vectors indicate movement from a reference macroblock to a current macroblock. In particular, a motion vector specifies where to retrieve a macroblock from a previously decoded frame (i.e., designates the "reference macroblock") to predict the pixel values of a current macroblock.

The error terms and the motion vectors are then provided to a motion compensation circuit 112. The motion compensation circuit 112 employs a

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reference macroblock and the error terms and motion vector for a current macroblock to predict the pixel values for the current macroblock. Once the pixel values for the current macroblock are determined, the current macroblock is stored into a display buffer memory 114. From the display buffer memory 114, the macroblocks are provided to a display circuit 116. The display circuit 116 may perform other display-related operations prior to actually displaying the decoded video. For example, the display circuit 116 may include circuitry for performing 420 to 422 conversion, letterbox conversion or other display-related operations.

Turning now specifically to the display function, the rate of consuming the macroblocks for display is regular. That is, the display operates synchronously to a display clock. However, as alluded to above, the order in which the pictures are encoded in the video bitstream 102 are not necessarily the order in which the pictures are to be displayed. Furthermore, MPEG 2 provides that the order in which the fields of a B picture are encoded are not necessarily the order in which the fields are to be displayed. In particular, a "top field" of a B picture frame may be provided before a "bottom field" of the same B picture frame, or vice versa. As a result, video decoder systems typically include a display buffer memory 114 that is large enough to hold three complete reconstructed and predicted pictures -- an I picture, a P picture and a B picture.

However, memory for three complete pictures does not come without cost. Because modern video decoder systems are typically employed in portable apparatuses such as DVD players, it is expensive in terms of power and space to provide memory. Furthermore, it is desirable to free up display buffer memory so that other memory-intensive operations may utilize the freed-up memory.

Summary

In accordance with the invention, a decoder system is provided for decoding an input video signal. A buffer memory hold slices of

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reconstructed B-pictures for display. The decoder is controlled in accordance with an amount of available memory in the buffer (the amount of available memory in the buffer depends both on how much data has been decoded and also upon how much data has been displayed). In addition, a buffer memory input controller controls into which locations of the buffer memory the slices of the reconstructed B-pictures are stored. As a result, only 2.53 frames of buffer memory are required.

Brief Description of the Figures

Fig. 1 illustrates a prior art decoding system.

Fig. 2 illustrates a decode synchronization circuit in accordance with an embodiment of the invention.

Fig. 3 is a flowchart that illustrates the processing of the display handling module of the Fig. 2 decode synchronization circuit.

Fig. 4 is a flowchart that illustrates the processing of the decode handling module of the Fig. 2 decode synchronization circuit.

Figs. 5A through 5C illustrate three different B picture decode and display schemes.

Figs. 6A through 6J illustrate an example of the decode and display scheme illustrated in Fig. 5C.

Fig. 7 shows a procedure in the "parse_upper_layer_RES" routine in Appendix A, that is executed once per field.

Fig. 8 shows a procedure in the "vid_field_init" routine in Appendix A, that is executed once per field.

Detailed Description

In accordance with a preferred embodiment of the invention, a decode synchronizer circuit 200 is provided, for use with a decoder system such as the prior art system 100, shown in Figure 1. Broadly speaking, the decode synchronizer circuit 200 operates to synchronize the decoder 101 to the display function 116. In a preferred embodiment, the decode synchronizer

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circuit 200 consists of cooperating software modules being executed by a microprocessor.

The display handling module 202 of the decode synchronizer circuit 200 is now discussed with reference to the flow chart in Figure 3. Since the display of I and P pictures may be entirely conventional, the focus of the following discussion is on displaying B pictures. Referring now to Figure 3, at label S302 of the flowchart, the display handling module 202 provides to display function 116 a pointer to a next slice of a B picture in the display buffer 114 to be displayed. Then, at step S304, the display handling function 202 waits to be awakened by a signal 203 that is synchronized to the display function 116. Then, when the signal 203 is received, the display handling function 202 wakes up and executes step S306. At step 306, the display handling function 202 makes a "free space" request to free the memory in the display buffer 114 of the slice just displayed.

In response to the "free space" request from the display handling function 202, a buffer pointer handling function 204 returns to the display handling function 202 a pointer to a next slice to be displayed. Then, at step S302, the display handling function 202 provides to display function 116 the pointer which the display handling function 202 just received from the buffer pointer handling function 204 to the next slice to be displayed.

Meanwhile, a decode handling function 206 is being executed by the processor in accordance with the flow chart shown in Figure 4. At step S402, the decode handling function 206 determines, by querying the buffer pointer handling function 204, whether there is space in display buffer 114 for another decoded slice. If it is determined at step S402 that there is space in display buffer 114 for another decoded slice, then, at step S404, the decode handling function 206 requests a pointer to the space in display buffer 114 for decoded slices. Then, at step S406, the decode handling function 206 provides the pointer to the allocated space to decoder 101 to initiate a decode. Alternately, if it is determined at step S402 that there is no space for decoded slices, then the decode handling function 206, at step S408, stalls. After

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stalling, execution continues at step S402.

An example of how buffer pointer handling function 204 operates is now described with reference to Figures 5A through 5C. As discussed in the Background, in MPEG 2, it is permissible for the order of I, P or B pictures in a coded bit-stream to be different from the order in which the pictures are to be displayed. Figures 5A through 5C illustrate a situation where the bit-stream is decoded in I picture, then P picture, then B picture order, while the decoded pictures are displayed in I picture, B picture, and P picture order.

In each instance, the display is offset in time from the decode by 3 field display times. That is, a field of an I picture decoded in field time period f1 is displayed in field time period f4. Furthermore, both I pictures and P pictures may need to be referenced to decode later pictures in a group of pictures. Thus, a complete picture area is required for each of a decoded I picture and P picture. By contrast, B pictures are not needed for further reference. That is, B pictures are "fleeting" data and need not be saved for further reference. The invention takes advantage of this characteristic of B pictures to minimize the amount of area in the display buffer 114 required to buffer these B pictures.

Turning now to Figure 5A, this figure illustrates a situation where the B picture is decoded top field first, then bottom field. As, as shown in Figure 5A, a top field of a B picture (shown as B_t in Figure 5A) need only be held in display buffer 114 for one field time period, until it is displayed in field time period f6. Meanwhile, in field time period f6, as the slices of B_t are being consumed by the display function 116, the slices of bottom field (B_b) of the B picture can be stored into the areas of display buffer 114 that are being freed up by the consumed portions of B_t. Thus, in an ideal situation, only 2.5 picture area are required for display buffer 114. However, since the decoder 101 and the display function 116 cannot be perfectly synchronized, it is necessary to have a small amount of additional area in the display buffer 114 (i.e., in addition to the 2.5 pictures worth of area) to account for this "slop". In a preferred embodiment, this additional area is

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limited to .03 pictures, the amount of area required to hold one slice of decoded picture.

Referring now to Figure 5B, this figure shows a situation where the bottom field (B_b) of the B picture is decoded before the top field (B_t) of the B picture. However, the fields of the B picture must be displayed in reverse, that is, the top field of the B picture must be displayed before the bottom field of the B picture. Thus, as shown in Figure 5B, the bottom field, after being decoded, is buffered for display. By contrast, the top field is displayed as it is being decoded. Thus, only a small portion (in the preferred embodiment, one slice) of the top field need be buffered in the display buffer 114.

Figure 5C illustrates a situation where B pictures are decoded in frame format, rather than field format. That is, the slices of the top field and the slices of the bottom field are decoded by the decoder 101 in an interleaving fashion. Thus, referring specifically to Figure 5C, in field period f5, slices of both top fields and bottom fields must be buffered. Then, in frame period f6, top field slices are displayed by display function 116. Meanwhile, the decoder 101 continues to decode top fields and bottom fields in the interleaving fashion. At this point, (i.e., in frame period f6), as new top field and bottom field slices are decoded, they are stored into portions of the display buffer 114 that are freed up as slices of the top fields are displayed. Then, by the time frame period F7 is reached, all of the slices of the bottom field have been decoded and stored into display buffer 114. These bottom field slices are then displayed by display function 116 during frame period F7.

Figure 6A through 6J illustrate a simplistic example of how a B picture, whose top and bottom fields each have ten slices, is stored into display buffer 114 during frame periods f5 and f6. Figure 6A illustrates the state of the portion of display buffer 114 used for buffering B picture data, at the beginning of frame period f6. In particular, Figure 6A shows that display buffer 114 includes slices T1 through T6 of the top fields and slices B1

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though B5 of the bottom field.

In Figure 6B, slice T1 has been displayed and the portion of display buffer 114, freed up by the display of slice T1, is now occupied by slice B6.

In Figure 6C, slice T2 has been displayed and the space in display buffer 114 previously occupied by now-displayed slice T2 is now occupied by decoded slice T7.

In Figure 6D, slice T3 has been displayed and the portion of display buffer 114 previously occupied by now-displayed slice T3 is now occupied by decoded slice B7. This continues from Figure 6E through 6I until, at Figure 6J, slice T10 has been displayed and the portion of display buffer 114 for holding decoded B picture data now holds slices B1 through B10 of the bottom field of the just decoded B picture.

In accordance with a preferred embodiment, the granularity of the buffer 114 is 44 (rather than 11 as set forth in the simplistic example), where each buffer piece (1/44) contains 8 display lines.

Attached hereto as Appendix A is a code listing that illustrates an embodiment of the display handling module 202, the buffer pointer handling module 204, and the decode handling module 206. Appendix A is to be considered an integral portion of this patent application. Fig. 7 shows a procedure in the "parse_upper_layer_RES" routine in Appendix A, that is executed once per field. Fig. 8 shows a procedure in the "vid_field_init" routine in Appendix A, that is executed once per field.

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What is claimed is:

1. A decoder system (100) for decoding an input video signal (102), comprising:

a decoder circuit (104) that reconstructs I-pictures from encoded I-picture data in the input video signal (102) and, from the I-pictures and data in the input video signal (102) other than the encoded I-picture data and motion vectors in the input video signal (102), generates P-pictures and B-pictures;

a buffer memory (114) that includes a plurality of independently addressable locations into which slices of the I-pictures, P-pictures and B-pictures are stored;

a buffer memory output controller (116) that consumes the slices at a regular rate, vacating the locations at which the consumed slices had been stored, and provides the consumed slices to an output of the buffer memory (114);

a decoder controller (206) that controls a rate of decoding by the decoder circuit (104) responsive to an amount of data (space indication) in the buffer memory (114); and

a buffer memory input controller (204) that controls into which locations of the buffer memory (114) the slices of the reconstructed B-pictures are stored such that:

if a B-picture is provided from the decoder circuit (104) in a first field format including a top field (B_t) and a bottom field (B_b), with the top field (B_t) provided before the bottom field (B_b) (Fig. 5A),

the slices of the top field (B_t) are stored into locations of a B-picture portion of the buffer memory (114), and

after slices of the top field (B_t) are consumed by the buffer memory output controller (116), the slices of the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t);

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if a B-picture is provided from the decoder circuit (104) in a second field format including a top field (B_t) and a bottom field (B_b), with the bottom field (B_b) provided before the top field (B_t) (Fig. 5B),

the slices of the bottom field (B_b) are stored into locations of the B-picture portion of the buffer memory (114), and

the slices of the top field (B_t) are initially stored into locations of the B-picture portion of the buffer memory (114) other than those locations occupied by the slices of the bottom field (B_b), then

as slices of the top field (B_t) stored into the B-picture portion of the buffer memory (114) are consumed by the buffer memory output controller (116), the remaining slices of the top field (B_t) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t); and

if a B-picture is provided from the decoder circuit (104) in a frame format, with slices of a top field (B_t) intermixed with slices of a bottom field (B_b) (Fig. 5C),

some slices of the top field (B_t) and the bottom field (B_b) provided from the decoder are stored into locations of the B-picture portion of the buffer memory (114) never occupied by slices of the B-picture; and

other slices of the top field (B_t) and the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the B-picture.

2. A decoder system (100) for decoding an input video signal (102), comprising:

a decoder circuit (104) that reconstructs I-pictures from encoded

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I-picture data in the input video signal (102) and, from the I-pictures and data in the input video signal (102) other than the encoded I-picture data and motion vectors in the input video signal (102), generates P-pictures and B-pictures;

a buffer memory (114) that includes a plurality of independently addressable locations into which slices of the I-pictures, P-pictures and B-pictures are stored;

a buffer memory output controller (116) that consumes the slices, vacating the locations at which the consumed slices had been stored, and provides the consumed slices to an output of the buffer memory (114);

a buffer memory input controller (204) that controls into which locations of the buffer memory (114) the slices of the reconstructed B-pictures are stored such that:

if a B-picture is provided from the decoder circuit (104) in a first field format including a top field (B_t) and a bottom field (B_b), with the top field (B_t) provided before the bottom field (B_b) (Fig. 5A),

the slices of the top field (B_t) are stored into locations of a B-picture portion of the buffer memory (114), and

after slices of the top field (B_t) are consumed by the buffer memory output controller (116), the slices of the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t);

if a B-picture is provided from the decoder circuit (104) in a second field format including a top field (B_t) and a bottom field (B_b), with the bottom field (B_b) provided before the top field (B_t) (Fig. 5B),

the slices of the bottom field (B_b) are stored into locations of the B-picture portion of the buffer memory (114), and

the slices of the top field (B_t) are initially stored into locations of the B-picture portion of the buffer memory (114)

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other than those locations occupied by the slices of the bottom field (B_b), then

as slices of the top field (B_t) stored into the B-picture portion of the buffer memory (114) are consumed by the buffer memory output controller (116), the remaining slices of the top field (B_t) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t); and

if a B-picture is provided from the decoder circuit (104) in a frame format, with slices of a top field (B_t) intermixed with slices of a bottom field (B_b) (Fig. 5C),

some slices of the top field (B_t) and the bottom field (B_b) provided from the decoder are stored into locations of the B-picture portion of the buffer memory (114) never occupied by slices of the B-picture; and

other slices of the top field (B_t) and the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the B-picture.

3. A decoder system (100) as in claim 2, wherein the buffer memory controller consumes the slices at a regular rate.

4. A decoder system (100) as in claim 2, and further comprising:

a decoder controller (206) that controls a rate of decoding by the decoder responsive to an amount of data in the buffer memory (114).

5. A decoder system (100) for decoding an input video signal (102), comprising:

a decoder circuit (104) that reconstructs I-pictures from encoded I-picture data in the input video signal (102) and, from the I-pictures and data

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in the input video signal (102) other than the encoded I-picture data and motion vectors in the input video signal (102), generates P-pictures and B-pictures;

a buffer memory (114) that includes a plurality of independently addressable locations into which slices of the I-pictures, P-pictures and B-pictures are stored;

a buffer memory output controller (116) that consumes the slices, vacating the locations at which the consumed slices had been stored, and provides the consumed slices to an output of the buffer memory (114);

a buffer memory input controller (204) that controls into which locations of the buffer memory (114) the slices of the reconstructed B-pictures are stored such that

if a B-picture is provided from the decoder circuit (104) in a field format including a top field (B_t) and a bottom field (B_b), with the top field (B_t) provided before the bottom field (B_b) (Fig. 5A),

the slices of the top field (B_t) are stored into locations of a B-picture portion of the buffer memory (114), and

after slices of the top field (B_t) are consumed by the buffer memory output controller (116), the slices of the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t).

6. A decoder system (100) for decoding an input video signal (102), comprising:

a decoder circuit (104) that reconstructs I-pictures from encoded I-picture data in the input video signal (102) and, from the I-pictures and data in the input video signal (102) other than the encoded I-picture data and motion vectors in the input video signal (102), generates P-pictures and B-pictures;

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a buffer memory (114) that includes a plurality of independently addressable locations into which slices of the I-pictures, P-pictures and B-pictures are stored;

a buffer memory output controller (116) that consumes the slices, vacating the locations at which the consumed slices had been stored, and provides the consumed slices to an output of the buffer memory (114);

a buffer memory input controller (204) that controls into which locations of the buffer memory (114) the slices of the reconstructed B-pictures are stored such that

if a B-picture is provided from the decoder circuit (104) in a field format including a top field (B_t) and a bottom field (B_b), with the bottom field (B_b) provided before the top field (B_t) (Fig. 5B),

the slices of the bottom field (B_b) are stored into locations of the B-picture portion of the buffer memory (114), and

the slices of the top field (B_t) are initially stored into locations of the B-picture portion of the buffer memory (114) other than those locations occupied by the slices of the bottom field (B_b), then

as slices of the top field (B_t) stored into the B-picture portion of the buffer memory (114) are consumed by the buffer memory output controller (116), the remaining slices of the top field (B_t) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t).

7. A decoder system (100) for decoding an input video signal (102), comprising:

a decoder circuit (104) that reconstructs I-pictures from encoded I-picture data in the input video signal (102) and, from the I-pictures and data in the input video signal (102) other than the encoded I-picture data and

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motion vectors in the input video signal (102), generates P-pictures and B-pictures;

a buffer memory (114) that includes a plurality of independently addressable locations into which slices of the I-pictures, P-pictures and B-pictures are stored;

a buffer memory output controller (116) that consumes the slices, vacating the locations at which the consumed slices had been stored, and provides the consumed slices to an output of the buffer memory (114);

a buffer memory input controller (204) that controls into which locations of the buffer memory (114) the slices of the reconstructed B-pictures are stored such that

if a B-picture is provided from the decoder circuit (104) in a frame format, with slices of a top field (B_t) intermixed with slices of a bottom field (B_b) (Fig. 5C),

some slices of the top field (B_t) and the bottom field (B_b) provided from the decoder are stored into locations of the B-picture portion of the buffer memory (114) never occupied by slices of the B-picture; and

other slices of the top field (B_t) and the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the B-picture.

8. A buffer memory input controller (204) that controls into which locations of a buffer memory (114) slices of B-pictures reconstructed from an input video signal (102) are stored such that:

if a reconstructed B-picture is in a first field format including a top field (B_t) and a bottom field (B_b), with the top field (B_t) provided before the bottom field (B_b),

the slices of the top field (B_t) are stored into locations of a B-picture portion of the buffer memory (114), and

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after slices of the top field (B_t) are consumed from the buffer memory (114), the slices of the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t);

if a reconstructed B-picture is in a second field format including a top field (B_t) and a bottom field (B_b), with the bottom field (B_b) provided before the top field (B_t),

the slices of the bottom field (B_b) are stored into locations of the B-picture portion of the buffer memory (114), and

the slices of the top field (B_t) are initially stored into locations of the B-picture portion of the buffer memory (114) other than those locations occupied by the slices of the bottom field (B_b), then

as slices of the top field (B_t) stored into the B-picture portion of the buffer memory (114) are consumed from the buffer memory (114), the remaining slices of the top field (B_t) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the top field (B_t); and

if a reconstructed B-picture is provided in a frame format, with slices of a top field (B_t) intermixed with slices of a bottom field (B_b) (Fig. 5C),

some slices of the top field (B_t) and the bottom field (B_b) provided are stored into locations of the B-picture portion of the buffer memory (114) never occupied by slices of the B-picture; and

other slices of the top field (B_t) and the bottom field (B_b) are stored into the locations of the B-picture portion of the buffer memory (114) vacated by the consumed slices of the

BNSDOCID: <WO_____9842139A1_I_>

B-picture.

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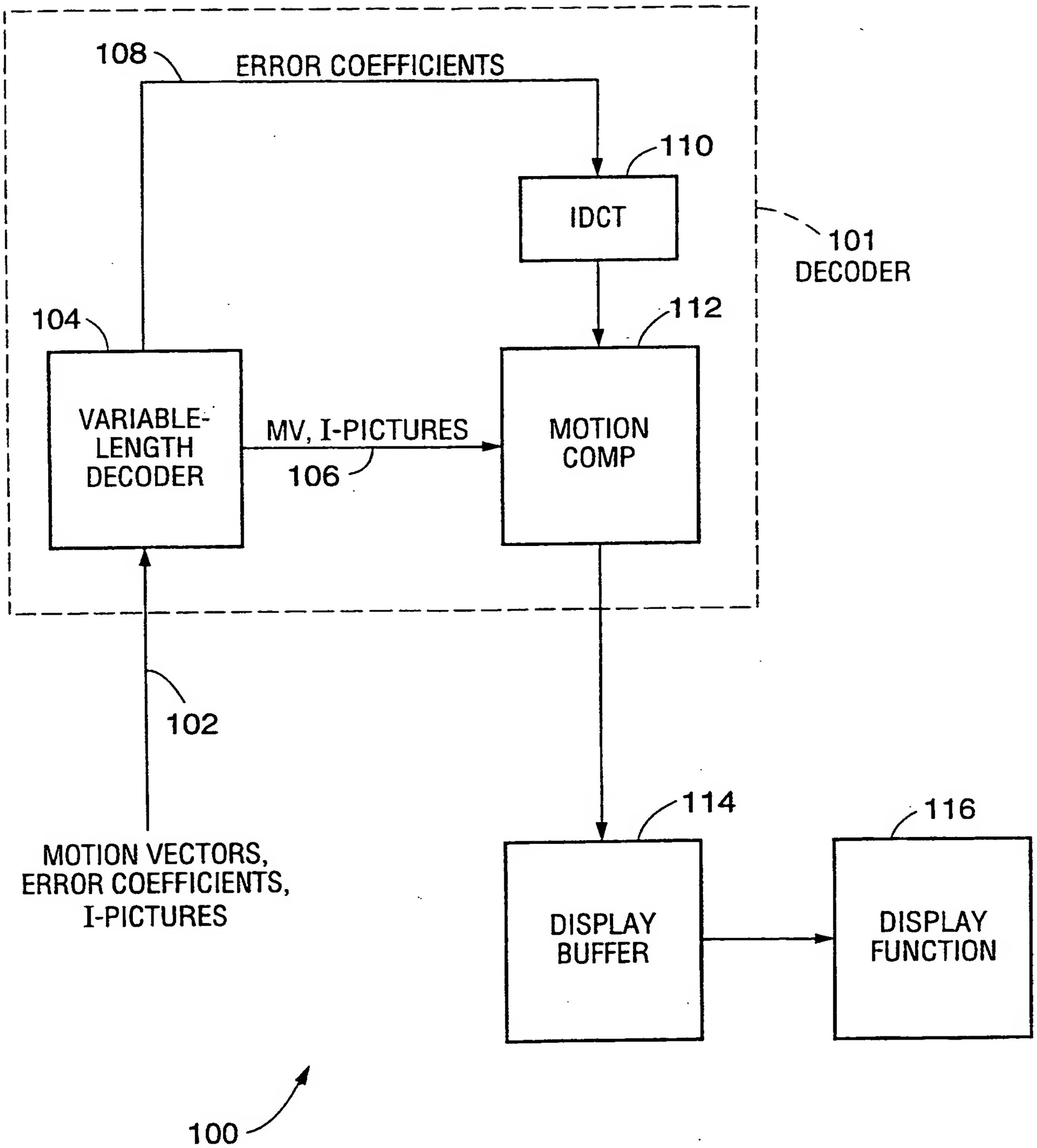

FIG. 1
(PRIOR ART)

BNSDOCID: <WO_____9842139A1_I_>

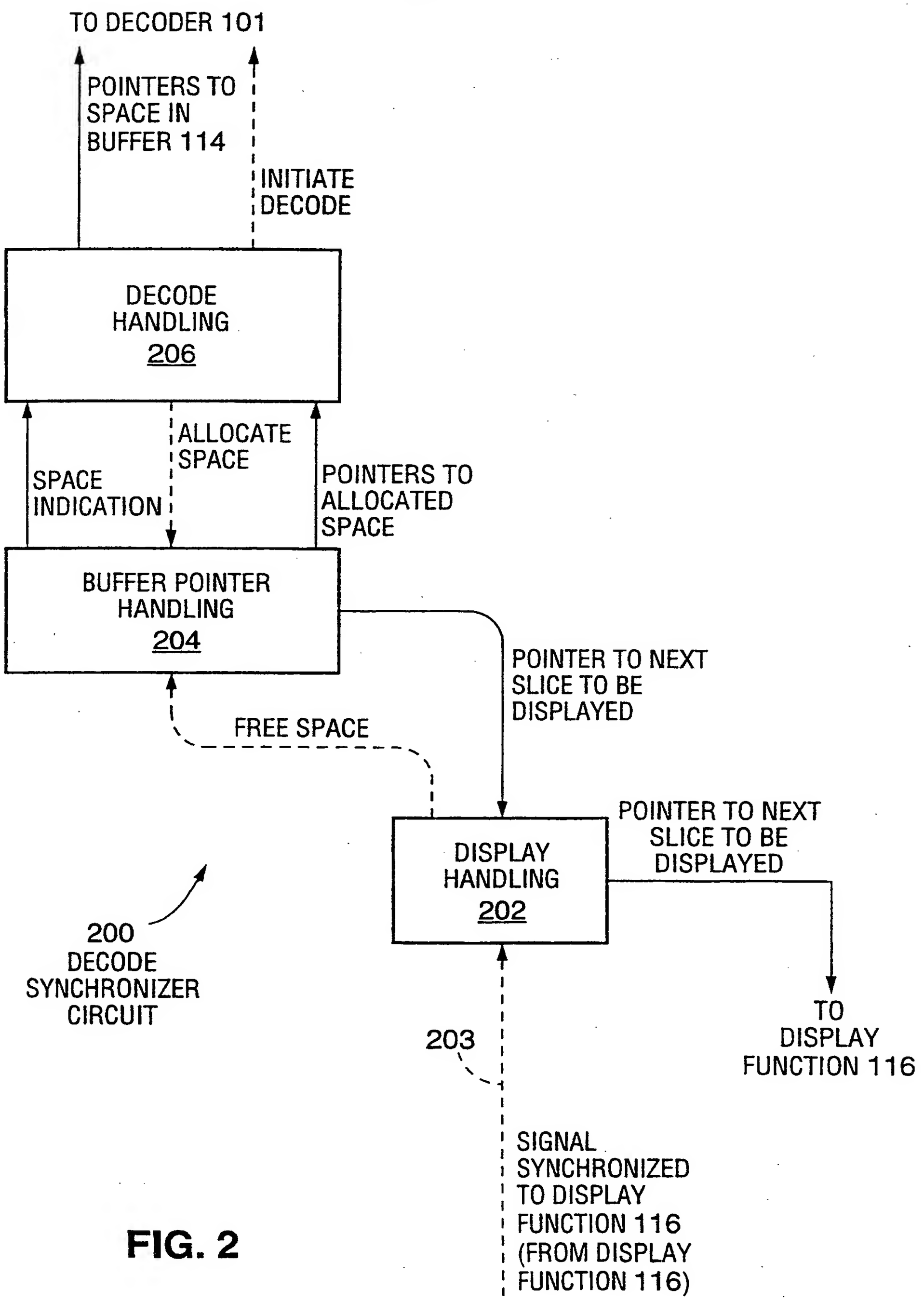

FIG. 2

BNSDOCID: <WO_____9842139A1_I_>

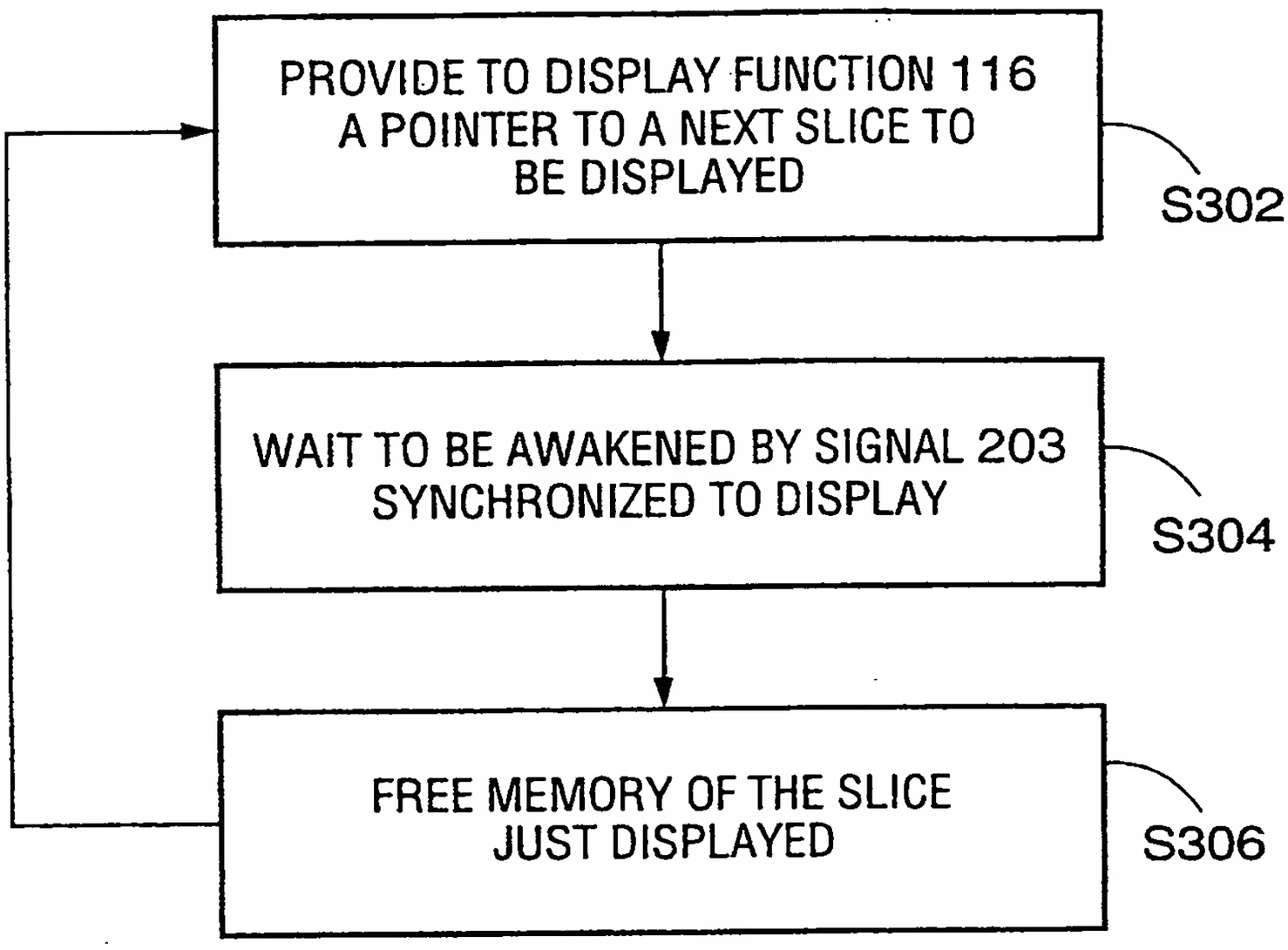

FIG. 3

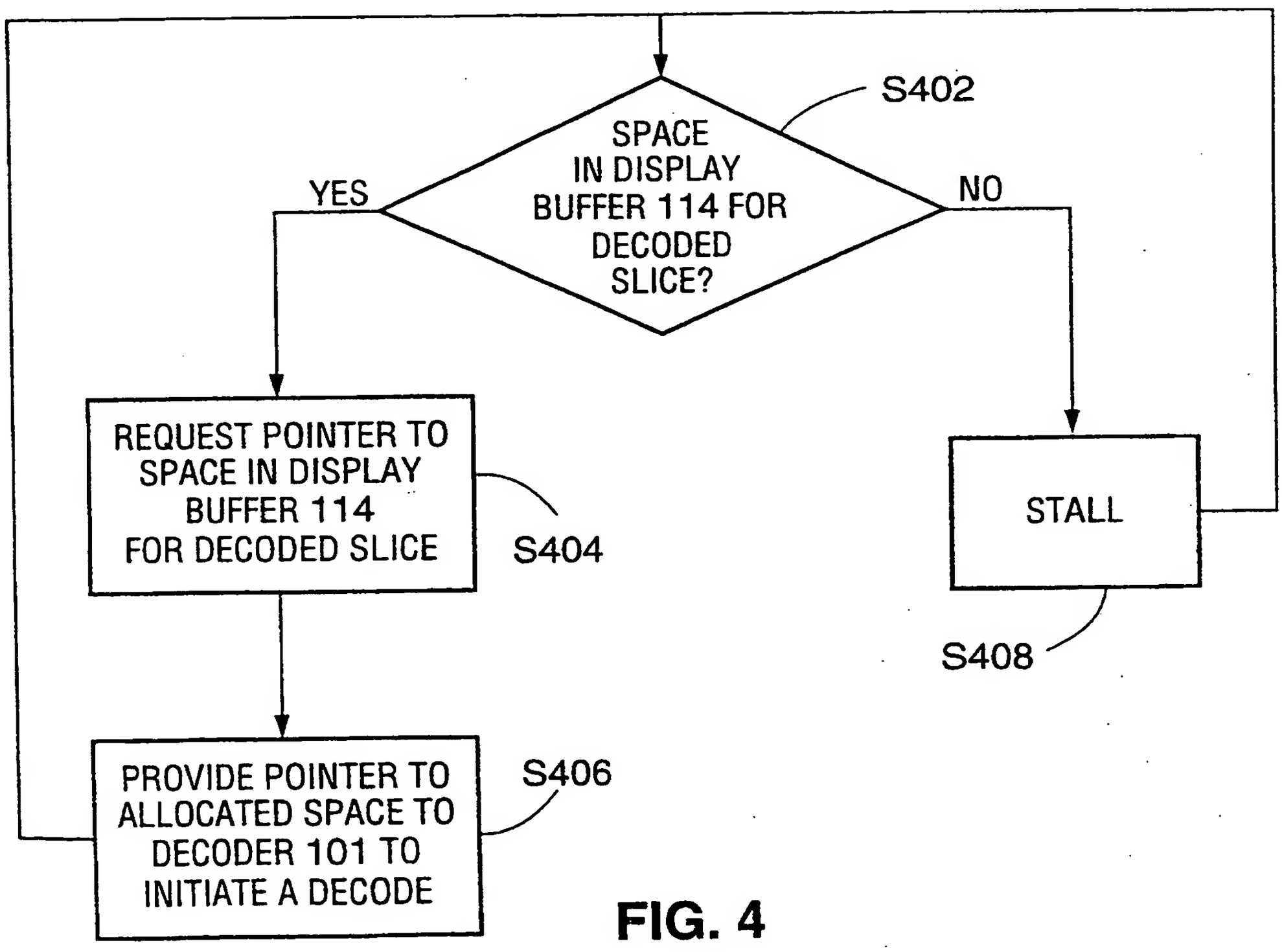

FIG. 4

BNSDOCID: <WO_____9842139A1_I_>

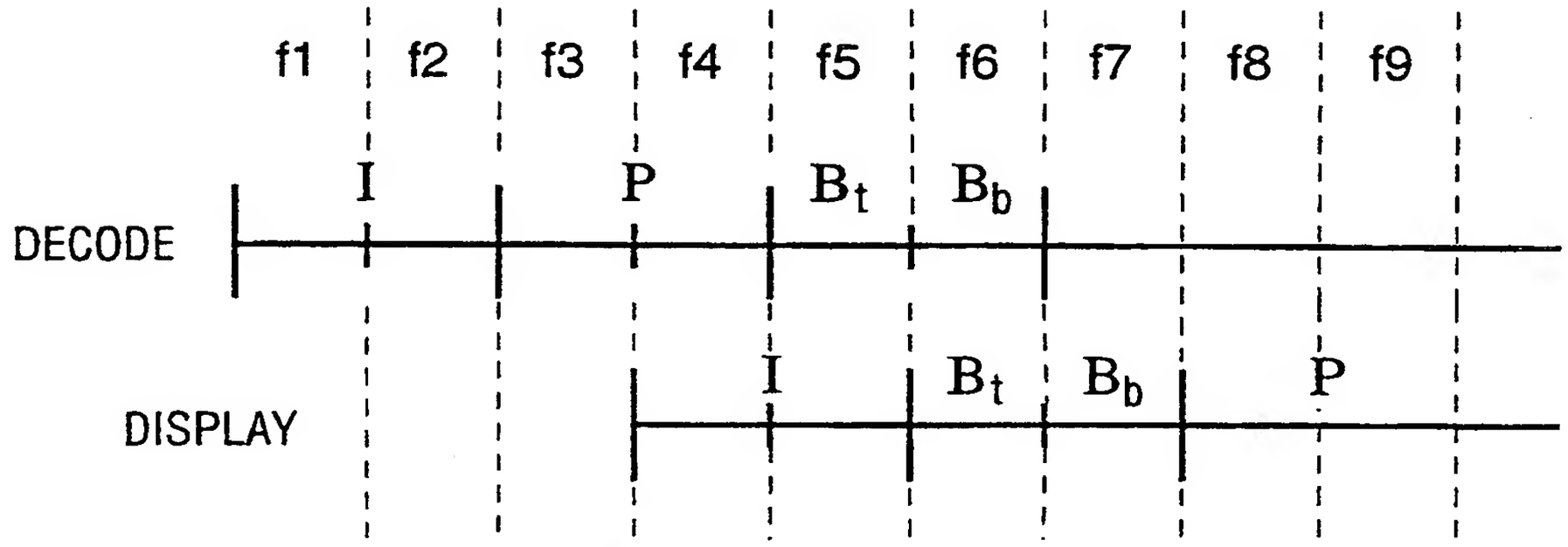

FIG. 5A

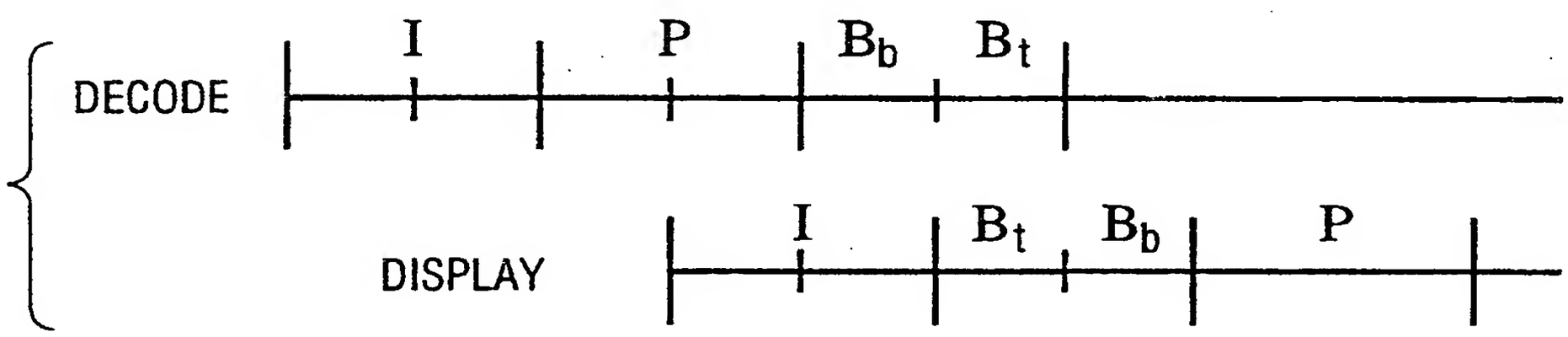

FIG. 5B

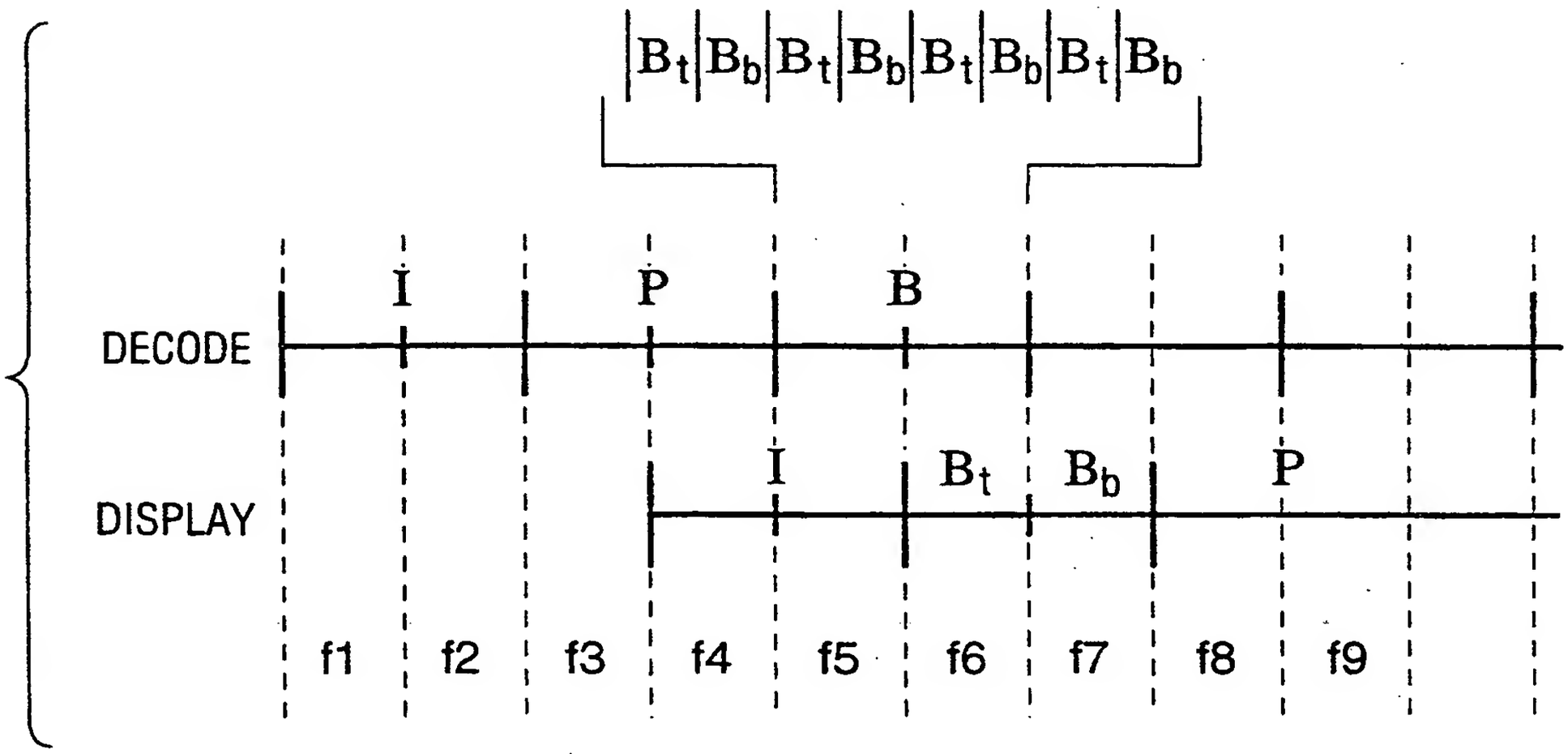

FIG. 5C

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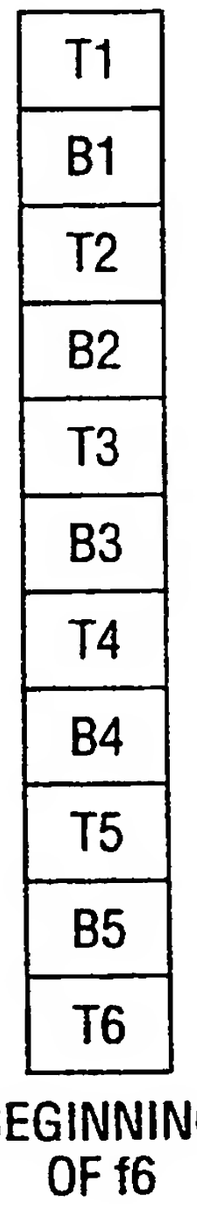
FIG. 6A



BEGINNING OF f6

FIG. 6B

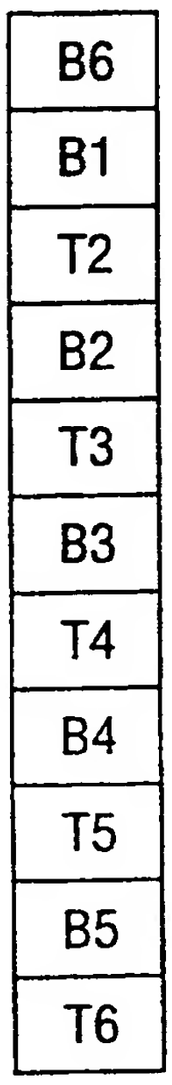


FIG. 6C

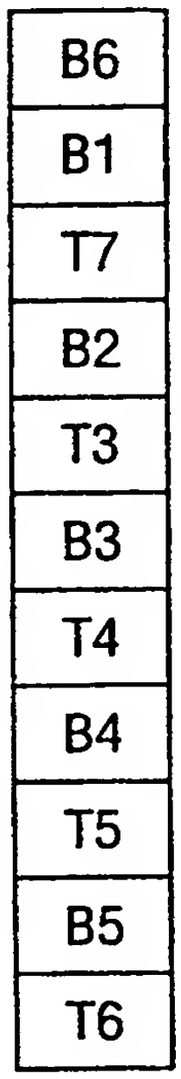


FIG. 6D

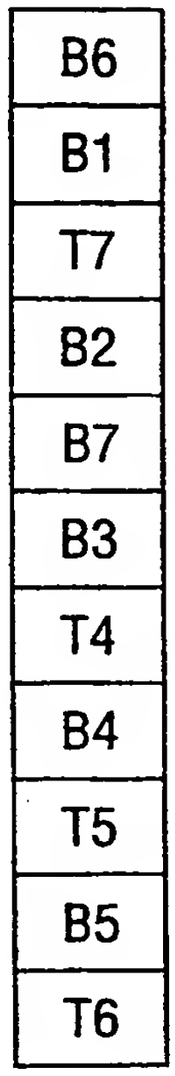


FIG. 6E

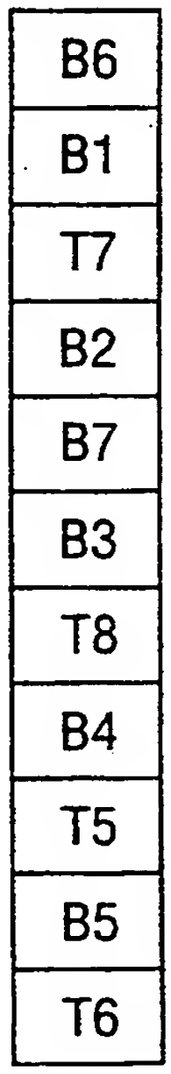


FIG. 6F

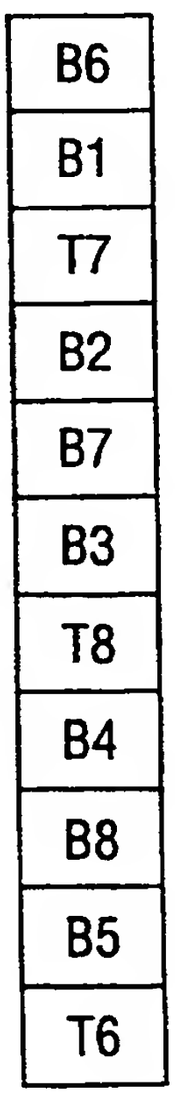


FIG. 6G

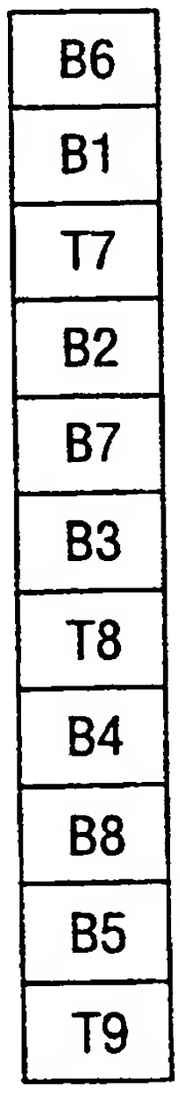


FIG. 6H

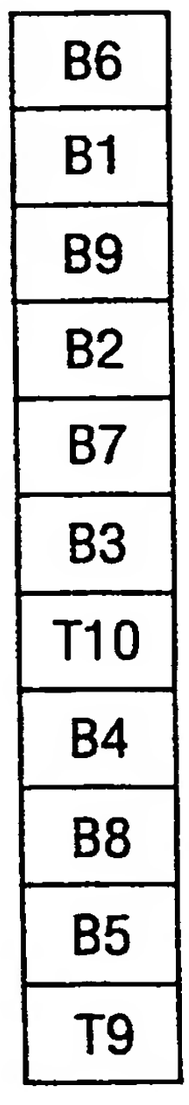


FIG. 6I

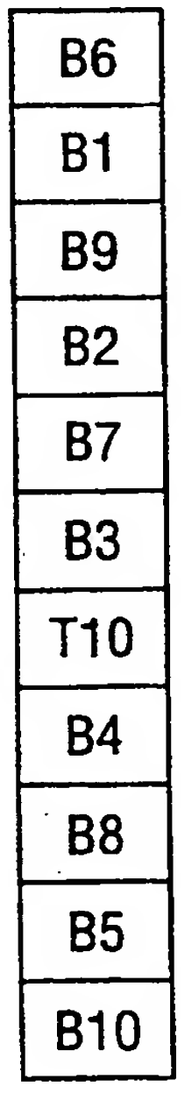
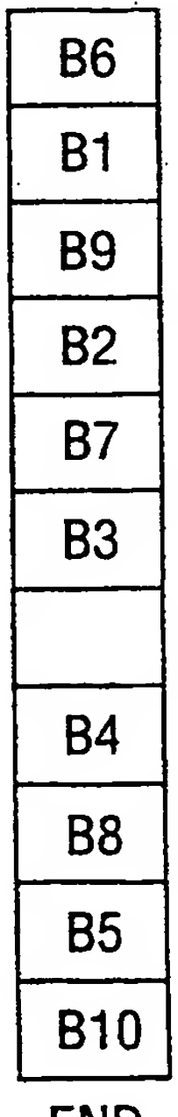


FIG. 6J



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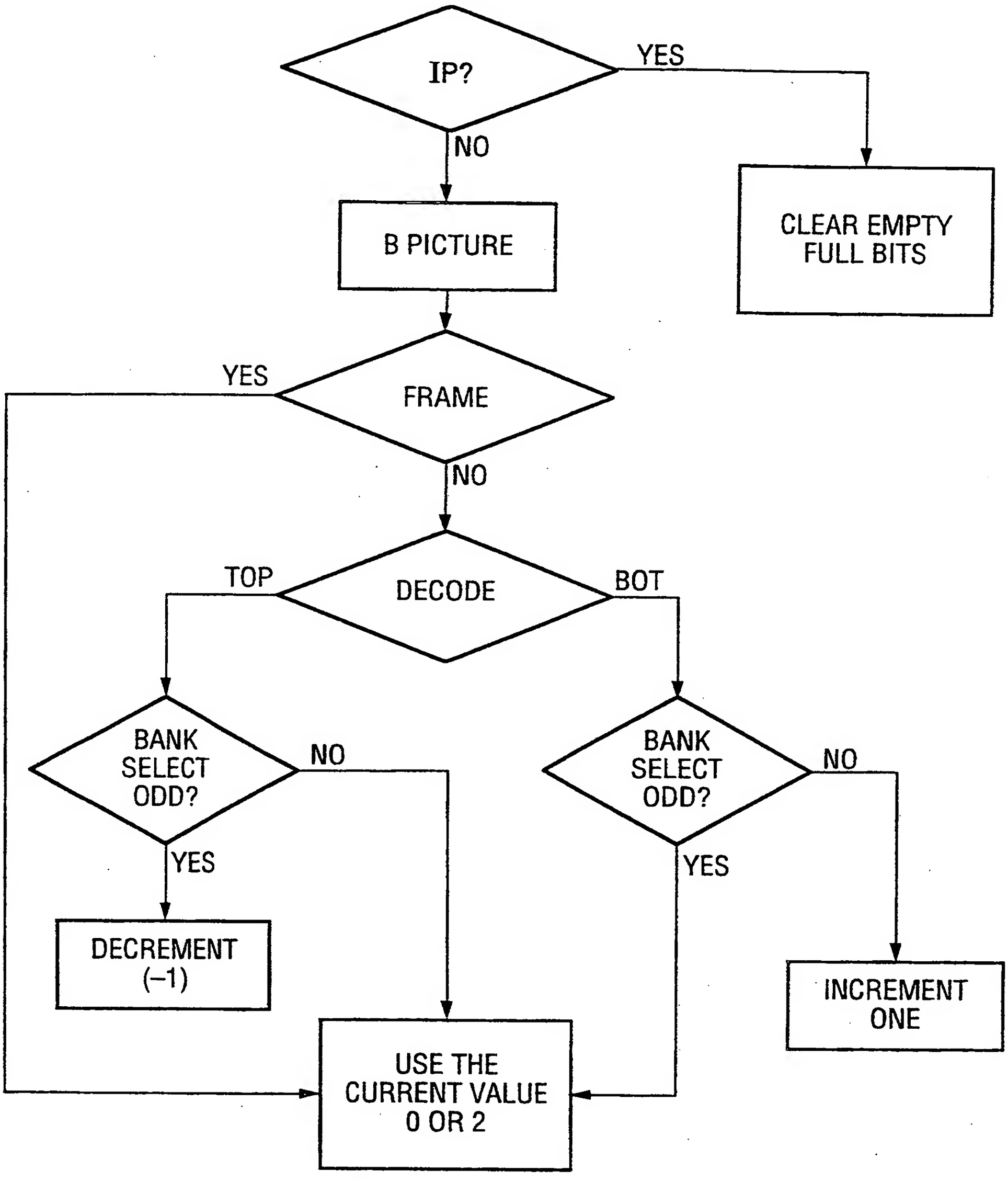

FIG. 7

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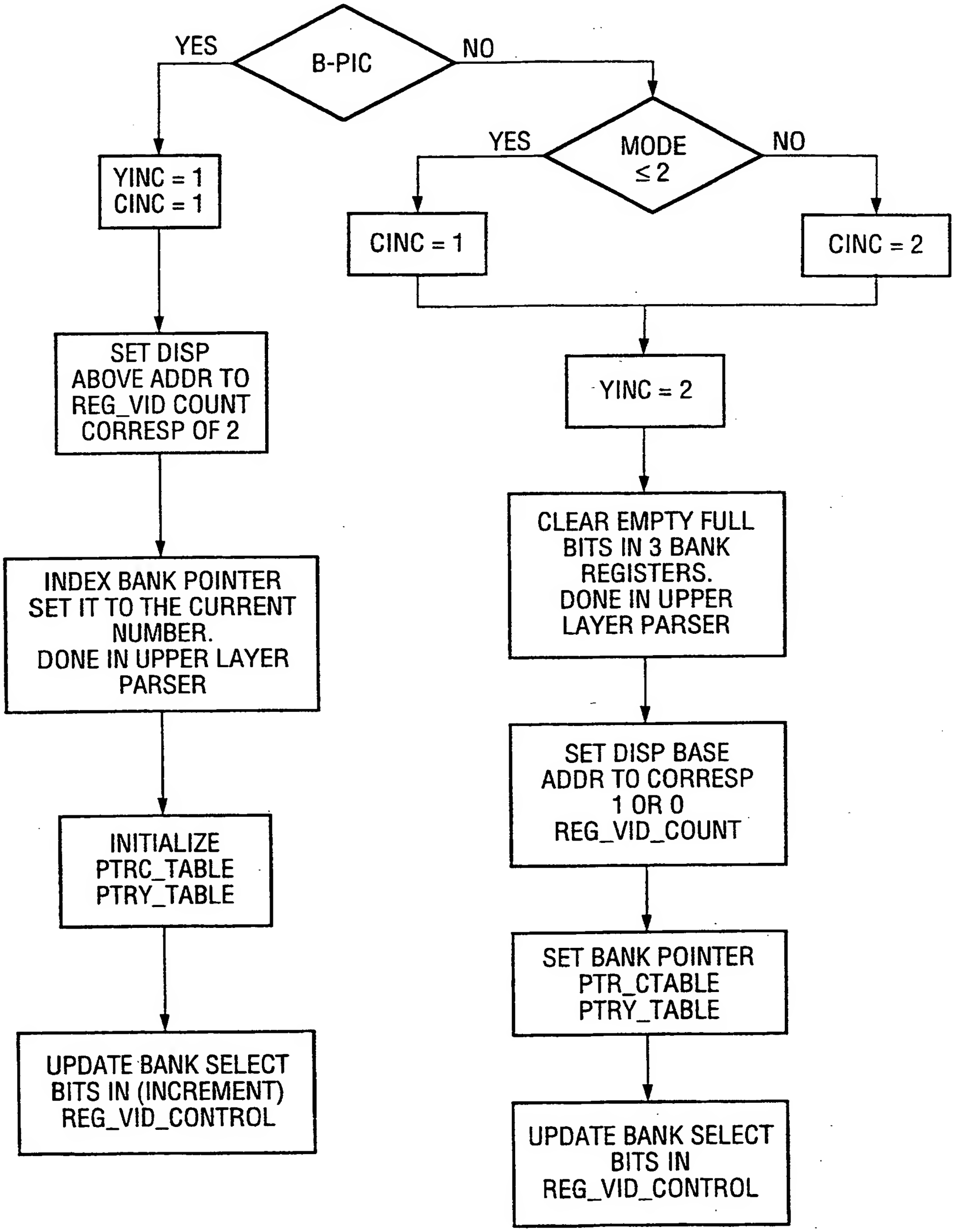

FIG. 8

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INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 98/04791

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N7/50

According to International Patent Classification(IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 618 722 A (PHILIPS ELECTRONIQUE LAB ;PHILIPS NV (NL)) 5 October 1994 see column 1, line 58 - column 2, line 29 see column 4, line 58 - column 5, line 5 see column 7, line 9 - line 25 see column 8, line 47 - column 9, line 5 see figure 4	1-8
X	WO 96 14710 A (COMPCORE MULTIMEDIA INC) 17 May 1996 see page 20, line 1 - line 34; table 4 see page 29, line 9 - page 30, line 26	1-8
P,X	GB 2 316 824 A (LG ELECTRONICS INC) 4 March 1998 see page 19, line 18 - page 21, line 6 see page 14, line 2 - line 5	1-3,5-8
P,A	see claims 29-35	4

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search	Date of mailing of the international search report
12 June 1998	23/06/1998

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Int ional Application No
PCT/US 98/04791

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication.where appropriate, of the relevant passages	Relevant to claim No.
P,X	EP 0 793 391 A (SGS THOMSON MICROELECTRONICS) 3 September 1997 see page 3, line 18 - line 52 see page 5, line 14 - line 22 see page 6, line 2 - line 3 see page 7, line 19 - line 49 see page 8, line 15 - line 23	1-3,5-8
P,A	see figures 4,5,7	4
A	EP 0 729 276 A (HITACHI LTD) 28 August 1996 see column 8, line 55 - column 10, line 34	1-8

1

BNSDOCID: <WO_____9842139A1_I_>

INTERNATIONAL SEARCH REPORT

Information on patent family members

In itional Application No
PCT/US 98/04791

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